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programmable logic device (PLD) bandwidth, including. core processing, embedded memory, routing, and I/O ... standard for a **boundary-scan**-based in-system ...
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JTAG **Boundary Scan** (IEEE 1149) is a unified scan-based. methodology for testing chips at the ... **Programmable Logic Device**. An IC that is programmed to ...
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Samples are artificially generated and in no way represent ...
Did much work with **Boundary Scan** JTAG test development. ... low frequency VCO design; Altera MAX+II design tools for PLD **Programmable Logic Device** design. ...
www.portnov.com/keyboard/analogmixedsignal.htm - 113k - Cached - Similar pages

Terms and Definitions
A **programmable logic device** which consists of an AND array forming logical products ... A finite state machine used to control the **boundary scan** interface. ...
www-ece.engr.ucf.edu/~jza/glossary/terms.html - 273k - Cached - Similar pages

EP patents matching keyword 'circuit'
EP531158, Method of and apparatus for encryption and **decryption** of communication ... EP640920, **Boundary-scan**-based system and method for test and diagnosis. ...
gauss.bacon.su.se/indices/keyword/25/ - 513k - Jun 19, 2005 - Cached - Similar pages

EP patents matching keyword 'program'
EP607657, **Programmable logic device** and method of operation ... EP464562, Method and apparatus for **decryption** of an information packet having a format ...
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Ñîääðæàíèå. Altera Digital Library 2002
AN 39 IEEE 1149.1 (JTAG) **Boundary-Scan** Testing in Altera Devices ... FLEX 8000 **Programmable Logic Device** Family Data Sheet ...
www.elcomcd.webhost.ru/altera/altera_toc.html - 39k - Cached - Similar pages

abklex.html
... Software/System Design/Distribution: BSDL **Boundary Scan** Description ... CPLD CMOS **Programmable Logic Device**: CPLD Complex **Programmable Logic Device** ...
www.ciw.uni-karlsruhe.de/abklex.html - 469k - Cached - Similar pages

EP patents published 1995
EP640920, **Boundary-scan**-based system and method for test and diagnosis. ...

EP679978, Method and apparatus enabling software trial using a **decryption** stub. ...
patent.tange.dk/ziki/indices/year/1995/ - 394k - Cached - Similar pages

Web Results **11** - **20** of about **46** for **"programmable logic device" "boundary scan" decryption**. (**0.06** secor

EP patents published 1993
EP523438, Microcomputer with **boundary-scan** facility. ... EP531158, Method of and apparatus for encryption and **decryption** of communication data. ...
patent.tange.dk/ziki/indices/year/1993/ - 384k - Cached - Similar pages
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[XLS] Acronyms
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Boundary-Scan Description Language (software) ... Encryption-**Decryption**-Envryption ... High-Capacity **Programmable-Logic Device** ...
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[PDF] Reconfigurable Logic: A Saviour for Experimental Computer ...
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Problem diagnosis and **boundary scan** testing is facilitated through support ... APEX 20K **Programmable Logic Device** Family Data Sheet. ...
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Abkuerzungsliste ABKLEX (PC-Format) W. Alex, Universitaet ...
... Software/System Distribution BSDL **Boundary Scan** Description Language BSF Bit ... CMOS **Programmable Logic Device** CPLD Complex **Programmable Logic Device** ...
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Dictionary Contents: all
... bounce; bounce message; **boundary scan**; boundary value analysis; bounded; ... complexity measure; complex number; complex **programmable logic device**; ...
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... CPLD CMOS **Programmable Logic Device** CPLD Complex **Programmable Logic Device** ... Display Manager GDE Generic **Decryption** Engine GDF Geographic Data Format ...
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CPLD – Configurable **Programmable Logic Device**. CPU – Central Processing Unit ... comunica-se com os pinos **Boundary Scan** da placa de prototipação. ...
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... bounce message **boundary scan** boundary value analysis bounded boundedly complete ... complex number complex **programmable logic device** component component ...
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JTAG: Definition and Much More From Answers.com
Who is...What is... Get 1-Click Answers. JTAG. Technology. JTAG (Joint Test Action

Group) An IEEE standard for **boundary scan** technology. See scan technology. ...
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"programmable logic device" "bound Search

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Good Advice .
... bounce bounce message **boundary scan** boundary value ... number complex **programmable logic device** component component ... Petri Net decompress **decryption** DECstation DECT ...
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... together with the current FLEX 8000 **Programmable Logic Device** Family and ... transformation filters, video formatters, and encryption/ **decryption** circuits—the ...
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... and other applications, such as encryption and **decryption**, and digital ... do you get it into the **programmable-logic device** or, for ... **BOUNDARY SCAN** TAP CONTROLLER ...
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... Logic Data Book, which describe device- specific information on Xilinx device characteristics, including readback, **boundary scan**, configuration, length count ...
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[PDF] Virtex-II Pro and Virtex-II Pro X FPGA User Guide
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Page 1. R Virtex-II Pro and Virtex-II Pro X FPGA User Guide UG012 (v3.0) 5 August 2004 Page 2. Virtex-II Pro and Virtex-II Pro X FPGA User Guide ...
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203.178.142.133/rg/2003f/bachelor-presen/paper/nn.pdf - Supplemental Result - Similar pages

[PDF] MDC IP CDP FPGA
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... CPLD – Configurable **Programmable Logic Device** CPU – Central Processing Unit DCR – Device Control Register DES – **Decryption**/Encryption System ...
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[PDF] Glossary
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... **Boundary Scan** JTAG **Boundary Scan** (IEEE 1149) is a unified scan-based methodology for testing chips at the board and system level. ...
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"programmable logic device" "bound Search

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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	18989	(pld or "programmable logic device")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/21 10:40
L2	757	l1 same ("boundary scan" or scan$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/21 10:41
L3	86	l2 same (decrypt$3 or decipher$3 or decod$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/21 10:50
L4	16	l3 same jtag	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/21 10:51
L5	308	l2 and (decrypt$3 or decipher$3 or decod$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/21 10:51
L6	48	l5 and jtag	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/21 10:51
L7	22	l2 and (decrypt$3 or decipher$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/21 12:02
L8	2	l7 and jtag	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/21 11:59
L9	3123	(trimberger.inv. or pang.inv. or thendean.inv.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/21 12:00

L10	4	l9 and l2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/21 12:02
L11	0	l10 and (decrypt$3 or decipher$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/21 12:02

Terms used **programmable logic device boundary scan decryption**

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Relevance scale

1 ICEBERG: an embedded in-circuit emulator synthesizer for microcontrollers
Ing-Jer Huang, Tai-An Lu
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**
Full text available: pdf(705.18 KB) Additional Information: full citation, references, citings, index terms

2 Evaluation of FPGA resources for built-in self-test of programmable logic blocks
Charles Stroud, Ping Chen, Srinivasa Konala, Miron Abramovici
February 1996 **Proceedings of the 1996 ACM fourth international symposium on Field-programmable gate arrays**
Full text available: pdf(49.07 KB) Additional Information: full citation, references, citings, index terms

3 Novel technique for testing FPGAs
C. Metra, G. Mojoli, S. Pastore, D. Salvi, G. Sechi
February 1998 **Proceedings of the conference on Design, automation and test in Europe**
Full text available: pdf(101.12 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

This paper presents a novel technique for testing Field Programmable Gate Arrays (FPGAs), suitable to be used in case of frequent FPGA reuse and rapid dynamic modifiability of the implemented function.

Keywords: Field Programmable Gate Arrays, testing, diagnosis, reuse

4 Designing SoCs for yield improvement: Using embedded FPGAs for SoC yield improvement
Miron Abramovici, Charles Stroud, Marty Emmert
June 2002 **Proceedings of the 39th conference on Design automation**
Full text available: pdf(200.31 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we show that an embedded FPGA core is an ideal host to implement infrastructure IP for yield improvement in a bus-based SoC. We present methods for testing, diagnosing, and repairing embedded FPGAs, for which complete testability is achieved without any area overhead or performance degradation. We show how an FPGA core can provide embedded testers for other cores in the SoC, so that cores designed to be tested with external vectors can be tested with BIST, and the entire SoC can be ...

5 Diagnosing programmable interconnect systems for FPGAs
Fabrizio Lombardi, David Ashen, Xiaotao Chen, Wei Kang Huang
February 1996 **Proceedings of the 1996 ACM fourth international symposium on Field-programmable gate arrays**
Full text available: pdf(196.47 KB) Additional Information: full citation, references, citings, index terms

6 CRUSADE: hardware/software co-synthesis of dynamically reconfigurable heterogeneous real-time distributed embedded systems
Bharat P. Dave
January 1999 **Proceedings of the conference on Design, automation and test in Europe**
Full text available: pdf(59.35 KB) Additional Information: full citation, citings, index terms

Results 1 - 6 of 6

Results for "**(programmable logic devices<in>metadata) <and> (boundary scan<in>metadata)**" e-mail
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(programmable logic devices<in>metadata) <and> (boundary scan<in>metadata) >>

IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

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1. **An HDL approach to board-level BIST**
Alves, G.R.; Gericota, M.G.; Ramalho, J.L.; Ferreira, J.M.M.;
Design Automation Conference, 1993, with EURO-VHDL '93. Proceedings EURO-DAC
20-24 Sept. 1993 Page(s):410 - 415
AbstractPlus | Full Text: PDF(516 KB) IEEE CNF

2. **ISP, JTAG and more for the MAX architecture**
Abu-Lebdeh, Z.M.;
WESCON/'95. Conference record. 'Microelectronics Communications Technology Proc
Products Mobile and Portable Power Emerging Technologies'
7-9 Nov. 1995 Page(s):200
AbstractPlus | Full Text: PDF(372 KB) IEEE CNF

3. **BIST for 1149.1-compatible boards: A low-cost and maximum-flexibility solution**
Ferreira, J.M.M.; Gericota, M.G.; Ramalho, J.L.; Alves, G.R.;
Test Conference, 1993. Proceedings., International
17-21 Oct. 1993 Page(s):536 - 543
AbstractPlus | Full Text: PDF(612 KB) IEEE CNF

4. **Proceedings of WESCON '94**
WESCON/94. 'Idea/Microelectronics'. Conference Record
27-29 Sept. 1994
AbstractPlus | Full Text: PDF(20 KB) IEEE CNF

5. **A 90.7 MHz-2.5 million transistors CMOS CPLD with JTAG boundary scan and in-programmability**
Patel, R.; Myron Wong; Costello, J.; Reese, D.; Bocchino, V.; Chu, M.; Turner, J.;
Custom Integrated Circuits Conference, 1995., Proceedings of the IEEE 1995
1-4 May 1995 Page(s):507 - 510
AbstractPlus | Full Text: PDF(372 KB) IEEE CNF

6. **Customers' needs drive complex PLDs to in-system programmability (ISP)**
Moran, M.A.;
WESCON/'95. Conference record. 'Microelectronics Communications Technology Proc
Products Mobile and Portable Power Emerging Technologies'
7-9 Nov. 1995 Page(s):213
AbstractPlus | Full Text: PDF(460 KB) IEEE CNF

7. **Bridging fault extraction from physical design data for manufacturing test develc**
Stroud, C.E.; Emmert, J.M.; Bailey, J.R.; Chhor, K.S.; Nikolic, D.;
Test Conference, 2000. Proceedings. International

3-5 Oct. 2000 Page(s):760 - 769
AbstractPlus | Full Text: PDF(936 KB) IEEE CNF

Results for "(programmable logic device<in>metadata) <and> (encryption<in>metadata)" e-mail
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» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

Select Article Information

1. **Security enhancements for A5/1 without loosing hardware efficiency in future mc**
Komninos, N.; Honary, B.; Darnell, M.;
3G Mobile Communication Technologies, 2002. Third International Conference on (Cor
8-10 May 2002 Page(s):324 - 328
AbstractPlus | Full Text: PDF(449 KB) IEE CNF

2. **A CPLD-based RC4 cracking system**
Kundarewich, P.D.; Wilton, S.J.E.; Hu, A.J.;
Electrical and Computer Engineering, 1999 IEEE Canadian Conference on
Volume 1, 9-12 May 1999 Page(s):397 - 402 vol.1
AbstractPlus | Full Text: PDF(344 KB) IEEE CNF

3. **Distributed security schemes for networks**
Wunnava, S.V.; Lule, E.;
SoutheastCon 2001. Proceedings. IEEE
30 March-1 April 2001 Page(s):114 - 117
AbstractPlus | Full Text: PDF(304 KB) IEEE CNF

4. **Implementation of pipelined data encryption standard (DES) using Altera CPLD**
Teo Pock Chueng; Yusoff, Z.M.; Sha'ameri, A.Z.;
TENCON 2000. Proceedings
Volume 3, 24-27 Sept. 2000 Page(s):17 - 21 vol.3
AbstractPlus | Full Text: PDF(276 KB) IEEE CNF

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IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
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